What is claimed is:

1. In an electronic system, a system for margin testing one or more components of the computer system, comprising

a fault bypass module incorporated in said electronic system, said fault bypass module masking signals indicative of faults associated with one or more of said components during margin testing of said electronic system.

2. The margin testing system of claim 1, wherein said at least one of said faults corresponds to an operating parameter associated with at least one of said components crossing a selected threshold.

3. The margin testing system of claim 2, wherein said operating parameter is any of frequency, voltage or temperature.

4. The margin testing system of claim 1, further comprising:

a controller internal to said electronic system and in communication with said fault bypass module, said controller transmitting a command to said fault bypass module for initiating masking of said fault signals by said module.

5. The margin testing system of claim 1, wherein said fault signals comprise:

interrupt signals.

6. The margin testing system of claim 1, wherein said fault bypass module permits normal processing of said fault signals during normal operation of said electronic system.

7. The margin testing system of claim 4, further comprising:

a hardware monitor in communication with said controller and with at least one of said components, said hardware generating an fault signal in response to occurrence of a fault associated with said at least one component.

8. The margin testing system of claim 7, wherein said hardware monitor transmits said fault signal to said fault bypass module, said fault bypass module masking said received fault signal during margin testing of said electronic device.

9. The margin testing system of claim 1, further comprising:

a power control element in communication with said fault bypass module, said fault bypass module transmitting one of more of said fault signals to said power control element in absence of margin testing and masking said one or more fault signals during margin testing of said electronic system.

10. The margin testing system of claim 9, wherein said fault bypass module masks said fault signal by intercepting said fault signal and supplying to said power control element a signal indicative of absence of a fault indicated by said fault signal.

11. The margin testing system of claim 7, wherein said at least one component is a power rail, and said hardware monitor generates an interrupt signal in response to a voltage associated with said power rail varying from a nominal value by more than a selected threshold.

12. The margin testing system of claim 11, wherein said power control module lowers power applied to said voltage rail in response to said interrupt signal in the absence of margin testing.

13. The margin testing system of claim 1, wherein said fault bypass module comprises:

a programmable logic device programmed to provide masking of said fault signals.

14. The margin testing system of claim 7, further comprising

a temperature diode coupled to at least one of said components and said hardware monitor for measuring a temperature of said component and supplying said measured temperature to said hardware monitor.

15. The margin testing system of claim 7, wherein said fault bypass module intercepts a selected output signal of said at least one component and generates a simulated signal corresponding to said intercepted output signal for transmittal to said hardware monitor during margin testing of said component.

What is claimed is:

1. In an electronic system, a system for margin testing one or more components of the computer system, comprising

a fault bypass module incorporated in said electronic system, said fault bypass module masking signals indicative of faults associated with one or more of said components during margin testing of said electronic system.

2. The margin testing system of claim 1, wherein said at least one of said faults corresponds to an operating parameter associated with at least one of said components crossing a selected threshold.

3. The margin testing system of claim 2, wherein said operating parameter is any of frequency, voltage or temperature.

4. The margin testing system of claim 1, further comprising:

a controller internal to said electronic system and in communication with said fault bypass module, said controller transmitting a command to said fault bypass module for initiating masking of said fault signals by said module.

5. The margin testing system of claim 1, wherein said fault signals comprise:

interrupt signals.

6. The margin testing system of claim 1, wherein said fault bypass module permits normal processing of said fault signals during normal operation of said electronic system.

7. The margin testing system of claim 4, further comprising:

a hardware monitor in communication with said controller and with at least one of said components, said hardware generating an fault signal in response to occurrence of a fault associated with said at least one component.

8. The margin testing system of claim 7, wherein said hardware monitor transmits said fault signal to said fault bypass module, said fault bypass module masking said received fault signal during margin testing of said electronic device.

9. The margin testing system of claim 1, further comprising:

a power control element in communication with said fault bypass module, said fault bypass module transmitting one of more of said fault signals to said power control element in absence of margin testing and masking said one or more fault signals during margin testing of said electronic system.

10. The margin testing system of claim 9, wherein said fault bypass module masks said fault signal by intercepting said fault signal and supplying to said power control element a signal indicative of absence of a fault indicated by said fault signal.

11. The margin testing system of claim 7, wherein said at least one component is a power rail, and said hardware monitor generates an interrupt signal in response to a voltage associated with said power rail varying from a nominal value by more than a selected threshold.

12. The margin testing system of claim 11, wherein said power control module lowers power applied to said voltage rail in response to said interrupt signal in the absence of margin testing.

13. The margin testing system of claim 1, wherein said fault bypass module comprises:

a programmable logic device programmed to provide masking of said fault signals.

14. The margin testing system of claim 7, further comprising

a temperature diode coupled to at least one of said components and said hardware monitor for measuring a temperature of said component and supplying said measured temperature to said hardware monitor.

15. The margin testing system of claim 7, wherein said fault bypass module intercepts a selected output signal of said at least one component and generates a simulated signal corresponding to said intercepted output signal for transmittal to said hardware monitor during margin testing of said component.

16. The margin testing system of claim 1, wherein said electronic system comprises a computer system.

17. The margin testing system of claim 15, wherein said computer system is a computer server.

18. The margin testing system of claim 4, wherein said controller comprises:
a BMC

19. The margin testing system of claim 18, further comprising:
a communication bus for providing communication between said BMC and said fault bypass module.

20. The margin testing system of claim 19, wherein said communication bus is an I^2C-based bus.

21. The margin testing system of claim 20, wherein said I^2C bus is an IPMB.

22. In an electronic system, a system for margin testing one or more components of the computer system, comprising:
a fault bypass module incorporated in said electronic system, said fault bypass module masking signals indicative of faults associated with one or more of said components during margin testing of said electronic system,
an internal controller in communication with said fault bypass module for transmitting a command to said fault bypass module to initiate masking of said fault signals by said module.

23. The margin testing system of claim 22, wherein said controller is a BMC.

24. A method of masking faults during margin testing of an electronic system, comprising:
intercepting one or more signals indicative of faults associated with one or more components of said electronic system during margin testing thereof, and

masking said intercepted signals by generating signals indicative of absence of said faults.